WHAT IS CLAIMED IS:

1. A semiconductor storage device comprising:

a memory cell array including memory cells, and bit lines for transfer of data in the memory cells;

an amplifier circuit connected to the bit lines to amplify data in the memory cells;

a first switching element connected between the bit lines and the amplifier circuit;

a first reference voltage source which applies to the gate of the first switching element a voltage for controlling the first switching element;

a second switching element and a third switching element connected in series between the gate of the first switching element and the first reference voltage source, said second switching element and said third switching element being connected in parallel to each other;

a second reference voltage source which applies to the gates of the second and third switching elements a voltage for controlling the second and third switching elements; and

a first timing shift circuit connected between the gate of the third switching element and the second reference voltage source to delay the operation of the third switching element from the operation of the second switching element.

2. The semiconductor storage device according to claim 1, wherein the first timing shift circuit is an RC delay circuit which is composed of a first resistor and a first capacitor.

3. The semiconductor storage device according to claim 1, wherein the second and third switching elements are P-channel transistors,

wherein the second and third switching elements turn OFF when the gates thereof are connected to the

first reference voltage source, and

wherein the second and third switching elements turn ON when the gates thereof are connected to the second reference voltage source.

4. The semiconductor storage device according to claim 1, further comprising a feedback circuit to return the gate voltage at the gate of the first switching element back to the first timing shift circuit,

wherein the first timing shift circuit connects the second reference voltage source to the gate of the third switching element when the gate voltage exceeds a given set voltage.

5. The semiconductor storage device according to claim 4, wherein the first timing shift circuit includes:

a third reference voltage source having a voltage between the voltage of the first reference voltage source and the voltage of the second reference voltage source;

a fourth switching element connected between the gate of the third switching element and the third reference voltage source, said fourth switching element having a gate connected to the gate of the first switching element; and

a fifth switching element connected between the gate of the third switching element and the second reference voltage source, said fifth switching element having a gate connected to the gate of the first switching element and being opposite in conduction type from the fourth switching element,

wherein the set voltage is based upon the difference between the voltage of the third reference voltage source and the threshold voltage of the fourth switching element.

6. The semiconductor storage device according to claim 1, further comprising:

a voltage control circuit interposed between the gate of the second switching element and the second reference voltage source to adjust the voltage from the second reference voltage source.

7. The semiconductor storage device according to claim 2, further comprising:

a voltage control circuit interposed between the gate of the second switching element and the second reference voltage source to adjust the voltage from the second reference voltage source.

8. The semiconductor storage device according to claim 4, further comprising:

a voltage control circuit interposed between the gate of the second switching element and the second reference voltage source to adjust the voltage from the second reference voltage source.

9. The semiconductor storage device according to claim 6, wherein the voltage control circuit includes:

a sixth switching element interposed between the gate of the second switching element and the second reference voltage source, said sixth switching element having the gate and the drain connected to the gate of the second switching element.

10. The semiconductor storage device according to claim 9, wherein the voltage control circuit includes:

a seventh switching element connected between the source of the sixth switching element and the gate of the second switching element in parallel with the sixth switching element, said seventh switching element having a gate connected to the gate of the first switching element.

11. The semiconductor storage device according to claim 10, wherein the voltage control circuit further includes:

an eighth switching element interposed between the sixth switching element and the second reference voltage

source, said eighth switching element having a gate and a drain connected to the source of the sixth switching element and a source connected to the second reference voltage source.

12. The semiconductor storage device according to claim 11, wherein the voltage control circuit is connected between the source of the eighth switching element and the gate of the second switching element in parallel to the sixth and eighth switching elements, said voltage control circuit having a gate connected to the gate of the first switching element.

13. The semiconductor storage device according to claim 12, wherein the voltage control circuit includes a ninth switching element having a threshold value higher than that of the seventh switching element.

14. The semiconductor storage device according to claim 1, further comprising:

a third reference voltage source having a voltage between the voltage of the first reference voltage source and the voltage of the second reference voltage source;

a fourth reference voltage source having a voltage between the voltage of the second reference voltage source and the voltage of the third reference voltage source;

a tenth switching element connected between the third reference voltage source and the gate of the first switching element;

an eleventh switching element connected between the fourth reference voltage source and the gate of the first switching element; and

a second resistor connected between the eleventh switching element and the gate of the first switching element,

wherein the eleventh switching element is OFF when the tenth switching element is ON and the eleventh

switching element is ON when the tenth switching element is OFF.

15. The semiconductor storage device according to claim 14, wherein operations of the tenth switching element and the eleventh switching element are synchronized with a signal which activates the amplifier circuit.

16. The semiconductor storage device according to claim 1, further comprising:

a third reference voltage source having a voltage between the voltage of the first reference voltage source and the voltage of the second reference voltage source;

a fourth reference voltage source having a voltage between the voltage of the second reference voltage source and the voltage of the third reference voltage source;

a tenth switching element connected between the third reference voltage source and the gate of the first switching element;

an eleventh switching element connected between the fourth reference voltage source and the gate of the first switching element;

a twelfth switching element connected in parallel to the eleventh switching element between the fourth reference voltage source and the gate of the first switching element; and

a second timing shift circuit to delay the operation of the twelfth switching element from the operation of the eleventh switching element.

17. The semiconductor storage device according to claim 16, wherein the second timing shift circuit is an RC delay circuit composed of a second resistor and a second capacitor.

18. The semiconductor storage device according to claim 16, further comprising a feedback circuit to

return the gate voltage at the gate of the first switching element back to the second timing shift circuit,

wherein the second timing shift circuit connects the second reference voltage source to the gate of the third switching element when the gate voltage exceeds a given set voltage.

19. The semiconductor storage device according to claim 1, wherein a channel width of the second switching element is narrower than that of the third switching element.

20. The semiconductor storage device according to claim 16, wherein a channel width of the seventh switching element is narrower than that of the twelfth switching element.